applications, movement encoders, and far-field applications. An example of a far-field application is a video game controller or other free space pointing application.

One novel aspect of the sequential read-out circuit of the present invention is the provision of a sample circuit for each column of the array and a single amplifier that is shared by the columns. The sample circuit provides a sampling function. The photocells of different columns in a particular row are sampled at the same time by the sample circuit. The amplifier reads each column in a sequential manner. In this manner, the photocells of different columns in the same row are read.

The architecture of the present invention is particularly attractive for applications that employ medium sized arrays. For example, the architecture of the present invention may be implemented in an exemplary application, where the array includes sixty-four (64) rows and sixty-four (64) columns of photocells.

FIG. 4 is a flowchart illustrating the steps performed by the sequential read-out circuit 20 of FIG. 1. In step 410, the output of all the photocells in a first row (e.g., the photocells in row_1) is sampled (e.g., sampled onto a respective column sample circuit). In step 420, the sample circuits are removed from the respective columns so that the output of the photocells of the first row is held (e.g., held on each respective sample circuit). In step 424, the photocells of the first row are reset (e.g., reset with a predetermined internal voltage). In step 428, the current photocell is sampled and the difference between Vlight and Vreset is determined. In step 430, the integration capacitor is reset. In step 434, it is determined whether the last photocell in the row has bee processed. When it is determined that the last photocell in the row has been processed, processing proceeds to step 444, where the the next row is processed (e.g., a row index is incremented). It is noted that steps 410 to 434 are then repeated for each row until all photocells have been processed.

When it is determined that the last photocell in the row has not yet been processed, processing proceeds to step 438, where the next photocell is processed (e.g., a column index is incremented). Processing then proceeds to step 428. Steps 428 to 438 are repeated for each photocell in a current row.

In processing step 428, photocells of the first row are sampled and the difference of each photocell is determined in a column-by-column fashion one photocell at a time. For example, the photocell in the first column of the first row is sampled. Specifically, when the photocell in the first column of the first row is sampled, the charge transfer circuit 30, which includes the integration capacitor, determines the difference between the first sampled voltage (e.g., Vlight) and the second voltalge level (Vreset) of the current photocell, thereby generating a voltage level that represents the amount of light received by the current photocell. The integration capacitor is then reset for the next photocell.

The photocell in the second column of the first row is then sampled. The charge transfer circuit 30, which includes the integration capacitor, determines the difference between the first sampled voltage (e.g., Vlight) and the second voltalge level (Vreset) of the current photocell, thereby generating a voltage level that represents the amount of light received by the current photocell. The integration capacitor is then reset for the next photocell. This sequence of steps is performed for all photocells in the row.

Processing then continues at step 410 where all the photocells in the next row are sampled onto the respective sample circuits.

The sample, hold, and convert stages are described in greater detail hereinafter.

Sample Stage

The amplifier has a reset mode and a charge transfer mode. During the reset mode of the amplifier, the column switches (e.g., first column switch and second column switch) are closed. In this regard, all photocells in a current row are sampled. For example, one side of each sample capacitor is tied to predetermined reference voltage (e.g., Vref) by virtue of the amplifier output being at Vref during unity gain mode. The second side of each sample capacitor is tied to the output voltage of a respective photocell (Vlight) through the output buffer N1 via the read transistor N2. In this stage, the output of all the photocells in a current row is sampled onto a respective column sample circuit (e.g., a respective column capacitor).

Hold Stage

In this stage, the column switches 148 are opened, and the charge information is held on the sampling capacitors. The photocells in the current row being read are reset to a starting voltage (Vreset). Since one side of the sampling capacitor (CSAMPLE) is open, none of the charge is disturbed from the original sampling.

Convert Stage

In this stage, the amplifier is placed into charge transfer mode. The first column is now connected to the amplifier via the column switch 148. The charge difference that moves the original voltage across the sample capacitor, Vlight-Vref to Vreset-Vref is transferred to the integration capacitor (CINT) of the amplifier, thereby causing a change in the output voltage equal to (Vlight-Vreset) *(CSAMPLE/CINT), which is the desired result. The output voltage is sampled by the down stream electronics. The integration capacitor (CINT) is then reset, and the sample capacitor (also referred to as the column capacitor) is removed.

The amplifier is placed into charge transfer mode, and the reading of the next column commences. After all the columns are read, the amplifier is left in reset, and the next row is sampled and then held. Then, the columns are converted one by one as described above.

Timing Diagram

FIG. 5 illustrates a timing diagram showing selected signals of FIG. 2. In this example, there are two rows and two photocells in each row. An amplifier reset signal 510 (TARST) is provided to reset the amplifier. The read signals 520 and 530 (i.e., READ_1 and READ_2) selectively switches the output transistors (transistor N2) in the photocells for the first and second rows, respectively. The reset signals 540 and 550 (i.e., RESET_1 and RESET_2) selectively connect the V_{light} nodes in the photocells for the first and second rows, respectively, to a predetermined voltage (e.g., V_{DD}). The sample signals 560 and 570 (i.e., SAMPLE_1 and SAMPLE_2) selectively connect the capacitors for the first and second columns to the negative input of the amplifier.